IN THE CLAIMS

Please amend the claims as follows:

1-16. (Canceled)

17. (Currently Amended) A memory cell, comprising:

a transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region, that are vertically aligned;

a trench capacitor ~~formed in a trench and coupled to the first source/drain region; and~~ having

a second plate of polycrystalline material formed in [[the]] a trench ~~that is coupled to~~ and a first plate integral with the second source/drain region ~~thereby~~ for forming a conductorless electrical connection between the trench capacitor and the transistor, the first plate having an etch-roughened surface, the second plate surrounds at least a portion of the first plate; and

an insulator layer that separates the second ~~polycrystalline~~ plate from the etch-roughened surface of the first plate , wherein the transistor further ~~including~~ includes a gate adjacent to the body region and the gate being vertically aligned with the second plate.

18. (Previously Presented) The memory cell of claim 17, wherein the second polycrystalline semiconductor plate comprises polysilicon.

19. (Currently Amended) The memory cell of claim 17, wherein the first plate comprises a heavily doped [[p-type]] n-type silicon substrate.

20-21. (Canceled)

22. (Currently Amended) A memory cell, comprising:

a vertical transistor formed outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region that are vertically aligned;

wherein a surface of the second source/drain region includes integral therewith a first plate having a polycrystalline surface layer that is etch-roughened;

a trench capacitor having a second plate that is formed in a trench that surrounds the first plate; and

wherein the first plate forms a conductorless electrical connection between the trench capacitor and the transistor, wherein the vertical transistor further ~~including~~ includes a gate adjacent to the body region and the gate being vertically aligned with the second plate.

23. (Previously Presented) The memory cell of claim 22, wherein the first plate integral with the second source/drain region comprises single crystalline silicon upon which is formed the layer of polysilicon .

24. (Canceled)

25. (Previously Presented) The memory cell of claim 22, wherein the second plate comprises polysilicon.

26. (Currently Amended) A memory device, comprising:

an array of memory cells, each memory cell including a vertical access transistor that is coupled to a trench capacitor wherein a first plate of the trench capacitor is integral with a second source/drain region so as to form a conductorless electrical connection between the trench capacitor and the vertical access transistor, the first plate including a micro-roughened surface layer of porous polysilicon, and a second plate of the trench capacitor disposed adjacent to the first plate and surround the first plate, wherein the vertical access transistor including a body region vertically aligned with the second source/drain region, and a gate adjacent to the body region, the gate being vertically aligned with the second plate;

a number of bit lines that are each selectively coupled to a number of the memory cells at a first source/drain region of the vertical access transistor;

a number of word lines disposed substantially orthogonal to the bit lines and coupled to gates of a number of vertical access transistors; and

a row decoder coupled to the word lines and a column decoder coupled to the bit lines so as to selectively access the cells of the array.

27. (Previously Presented) The memory device of claim 26, wherein the first plate comprises a single crystalline layer upon which is formed the layer of polysilicon .

28. (Canceled)

29. (Previously Presented) The memory device of claim 26, wherein the second plate comprises polysilicon.

30. (Canceled)

31. (Currently Amended) A memory cell, comprising:

a transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a second source/drain region ~~having a first plate formed integral therewith~~, a body region and a first source/drain region vertically aligned with the second source/drain region;

a trench capacitor ~~formed in a trench and~~ including a first plate ~~electrically~~ coupled to the second source/drain region without an intervening conductor ~~to the first plate~~, the first plate surrounds at least a portion of the second plate; and

wherein the trench capacitor further includes a polysilicon second plate formed in [[the]] a trench ~~that is coupled to the first plate of the second source/drain region~~, the first plate including a surface layer of polysilicon that is etch-roughened, and an insulator layer that separates the polysilicon second plate from the etch-roughened polysilicon surface of the first

plate, wherein the transistor further ~~including~~ includes a gate adjacent to the body region and the gate being vertically aligned with the polysilicon second plate.

32. (Currently Amended) The memory cell of claim 31, wherein the first plate comprises heavily doped [[p-type]] n-type silicon .

33. (Canceled)

34. (Currently Amended) A memory cell, comprising:

a vertical transistor formed outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region that are vertically aligned, wherein the second source/drain region includes integral therewith a single crystalline silicon first plate with a layer of polysilicon having an etch-roughened surface; and

a trench capacitor with a second plate that is formed in a trench and that surrounds at least the etch-roughened surface of the first plate; and

wherein the first plate forms a conductorless electrical connection between the trench capacitor and the transistor, wherein the vertical transistor further ~~including~~ includes a gate adjacent to the body region and the gate being vertically aligned with the second plate.

35. (Previously Presented) A memory device, comprising:

an array of memory cells, each memory cell including a vertical access transistor that is electrically connected without an intervening conductor to a trench capacitor by a first plate of the trench capacitor that is integral with a second source/drain region of the vertical access transistor, the first plate including a micro-roughened surface of porous polysilicon, with a second plate of the trench capacitor disposed so as to surround at least the micro-roughened surface of the first plate, wherein the vertical access transistor including a body region vertically aligned with the second source/drain region, and a gate adjacent to the body region, the gate being vertically aligned with the second plate;

a number of bit lines that are each selectively coupled to a number of the memory cells at a first source/drain region of the vertical access transistor;

a number of word lines disposed substantially orthogonal to the bit lines and coupled to gates of a number of vertical access transistors; and

a row decoder coupled to the word lines and a column decoder coupled to the bit lines so as to selectively access the cells of the array.

36. (Previously Presented) The memory device of claim 35, wherein the vertical access transistor includes a body region of p-type single crystalline silicon adjoining the second source/drain region, wherein the second source/drain region is n-type single crystalline silicon.

37. (Previously Presented) The memory cell of claim 31, wherein the second source/drain region is P-doped or N-doped.

38. (Canceled)

39. (Previously Presented) The memory cell according to claim 34, wherein the single crystalline polysilicon is P-doped or N-doped.

40. (Previously Presented) The memory cell according to claim 35, wherein the second source/drain of the vertical access transistor is P-doped or N-doped.

41. (Currently Amended) A memory cell, comprising:

a transistor comprising outwardly from a substrate a second source/drain region at least a portion of which serves as a single crystalline first capacitor plate for forming a conductorless connection of the transistor to a trench capacitor, a body region and a first source/drain region vertically aligned with the second source/drain region, wherein the first capacitor plate includes a micro-roughened surface for increasing the capacitance of the trench capacitor;

the trench capacitor being formed in a trench surrounding a portion of the transistor and including a second capacitor plate of polycrystalline material formed so as to surround the first capacitor plate; and

an insulator layer that separates the second polycrystalline semiconductor plate from the micro-roughened surface of the first plate, wherein the transistor further ~~including~~ includes a gate adjacent to the body region and the gate being vertically aligned with the second plate.

42. (Previously Presented) A memory cell according to claim 41, wherein the micro-roughened surface of the first capacitor plate comprises a layer of polysilicon.

43. (Previously Presented) The memory cell according to claim 41, wherein the second source/drain region that includes the first capacitor plate, the body region, and the first source/drain region are formed as a pillar of single-crystal semiconductor material.

44. (Previously Presented) The memory cell according to claim 41, wherein the second plate also surrounds first plates of adjacent memory cells.

45. (Previously Presented) The memory cell according to claim 44, wherein the second plate is grounded.

46. (Previously Presented) The memory cell according to claim 17, wherein the first plate also surrounds second plates of adjacent memory cells.

47. (Previously Presented) The memory device according to claim 26, wherein the second plate also surrounds first plates of adjacent memory cells.

48. (Previously Presented) The memory cell according to claim 31, wherein the second plate also surrounds first plates of adjacent memory cells.

49. (Canceled)

50. (Previously Presented) The memory device according to claim 35, wherein the second plate also surrounds first plates of adjacent memory cells.

51. (Canceled)

52. (New) A memory cell comprising:

a vertical transistor formed on a substrate, the vertical transistor including a first source/drain region, a body region, and a second source/drain region vertically aligned with the first source/drain region and the body region;

a trench capacitor including first plate being formed integrally with the second source/drain region, and a second plate formed in a trench that surrounds the first plate, the first plate having an etch-roughened surface, the second plate having top surface; and

a word line for activating the vertical transistor, the word line being formed above the top surface of the second plate.

53. (New) A memory device comprising:

an array of memory cells, each of the memory cells including a vertical transistor and a trench capacitor, the vertical transistor including a body region, a first source/drain region, and a second source/drain vertically aligned with the body region and the first source/drain region, the first plate including a micro-roughened surface of polysilicon, the trench capacitor including a first plate formed integrally with the second source/drain region, and a second plate formed in a trench that surrounds the first plate;

a plurality of word lines for activating the vertical transistor of each of the memory cells, each of the word lines being formed above a top surface of the second plate of trench capacitor; and

a plurality of bit lines, each of the bit lines is coupled to a selected a number of the memory cells at the first source/drain region of the vertical access transistor of each of the selected number of the memory cells,